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Document Title **CAL Front End (GCFE) ASIC – Version 5 Functional Test Report**		

GLAST LAT Calorimeter Front-End Electronics (GCFE) ASIC

Version 5 Functional Test Report

Document Approval

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Change History Log

Revision	Effective Date	Description of Change

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Applicable Documents:

1. LAT-PS-00567-D1, “GLAST CAL Analog Front-End (GCFE) ASIC Test Procedure”, Tammy Faulkner, January 30, 2002.

2. LAT-SS-00423-D4, “GLAST LAT Design Description of the GLAST Calorimeter Front-End Electronics (GCFE) ASIC (GCFE4 submission)”, W. Neil Johnson and James Ampe, November 28, 2001.

3. LAT-SS-00424-D2, “GLAST LAT Design Description of the GLAST Calorimeter Front-End Electronics (GCFE) ASIC (GCFE5 submission)”, W. Neil Johnson and James Ampe, November 28, 2001.

4. LAT-SS-00089-D2, “GLAST LAT GLAST Calorimeter Front-End Electronics (GCFE) ASIC Specification”, W. Neil Johnson, January 10, 2001.

5. LAT-SS-00208-D2, “Calorimter Readout Control ASIC – Conceptual Design”

Test Description

This document gives the test results from the execution of the GCFE ASIC Development Test Procedure as documented in item 1 above on the GCFE version 5 in comparison to version 4. This test exercises the functionality and evaluates the performance of the ASIC chip. Where possible, the functionality of individual sub-devices on the ASIC are exercised and verified. Complete data acquisition sequences are performed to confirm end-to-end functionality and to verify those sub-devices that cannot be individually tested. Finally, Energy Range, Noise, and Linearity measurements are made as a measurement of performance.

This test does not perform a complete evaluation of specification compliance. That test is a separate procedure yet to be defined and executed.

The units under test was a sample of the GCFE ASIC version 5 chips received at NRL. The testing was performed on NRL’s GCFE test board S/N 1. All tests were performed with the nominally defined Pre-Amp Gain settings of LE = 5, HE = 13, unless otherwise stated. The complete test data and results can be found in the executed test procedure and accompanying spreadsheets. These spreadsheets will be kept on-file on the NRL server.

Test Summary:

	LEX8		**LEX1**		**HEX8**		**HEX1**	
	Expected	**Measured**	**Expected**	**Measured**	**Expected**	**Measured**	**Expected**	**Measured**
ADC Noise (1-sigma)	< 2000 e-	2000 e-	< 2000 e-	3000 e-	< 2000 e-	2100 e-	< 2000 e-	2800 e-
Slow Shaper Noise (1-sigma)		2 mV		N/A		2 mV		N/A
Analog Out Noise (1-sigma)		9 mV		3 mV		9 mV		3 mV
Integral Non-linearity	+/- 0.5%	0.5 to -0.8 1.0 to -2.0	+/- 0.5%	0.5 to –0.9 0.5 to –0.5	+/- 0.5%	1.2 to 6.0 0.8 to –2.2	+/- 0.5%	0.5 to –1.5 0.3 to –1.0
Min Threshold	2 MeV		5 MeV		100 MeV		300 MeV	
Energy Range Upper Limit	200 MeV	101 MeV 172 MeV	1.6 GeV	921 MeV 887 MeV	12.8 GeV	1069 MeV 915 MeV	100 GeV	5842 MeV 5313 MeV
Fast Shaper Trigger Delay	0.5 +/- 0.2 µsec	0.19 – 0.70 usec			0.5 +/- 0.2 µsec	Not Functional		
Slow Shaper Peak Delay (msec)	3.5 +/-0.5 all w/i +/-0.2	Not Measured	3.5 +/- 0.5 all w/i +/- 0.2	Not Measured	3.5 +/- 0.5 all w/i +/- 0.2	Not Measured	3.5 +/- 0.5 all w/i +/- 0.2	Not Measured
Pre-Amp Gains	See table below							
Power Consumption	< 6 mW	Not Measured	< 6 mW	Not Measured	< 6 mW	Not Measured	< 6 mW	Not Measured

Where 2 results are listed, the first is SN 1 and the second is SN 2 of the 2 Version 5 ASICs tested.

Chip Functionality:

The chip write and Read functionality was verified to all registers after the command function bits were updated to the new settings as documented in LAT-SS-00208-D2, Table 3.

The low energy internal trigger capability was successfully tested. When the FLE_DAC setting was higher than x61, triggering occurred only during pulse events. Lower settings resulted in continuous pulses on signal noise. The results of the trigger timing measurements are presented below.

The high-energy internal trigger capability was un-successful. Regardless of trigger setting, continuous triggers occurred with and without signal input. A continuous trigger condition was observed on the HE_DISC lines.

The auto-range functionality worked in the same manner as was reported during Version 4 testing. Detailed measurements of the RNG_ULD_DAC settings have not been made yet.

The LOG_ACCEPT discriminator functionality was also successfully verified.

Noise Measurements:

Measurements were made using the calibration input for a single source and the MAX 145 ADC to read the analog output signal. The measurements were made in a minimal noise environment with the test board enclosed in a metal box without scope probes or other sources of noise.

The calibration DAC was stepped 100 steps over its range with 200 measurements taken at each step. The mean and standard deviation of each measurement were recorded to a spreadsheet. Once the ADC reading exceeds 2300 mV, the determined saturation point, the recording of measurements stop.

The Noise measurements in the plots below are the standard deviation of the 200 ADC measurements recorded for each step. The specification for this value is < 2000 e- for all channels. The LEX8 and HEX8 channels are, for the most part, within this specification. The LEX1 and HEX1 channels have a noise measurement of < 3000 e-. The improvement in noise from Version 4 to Version 5 is significant but it is unknown how much of this improvement is due to the biased voltage applied to the Version 5 ASICs.

Figure 1: Version 4 ADC Measurement Noise (1-sigma)

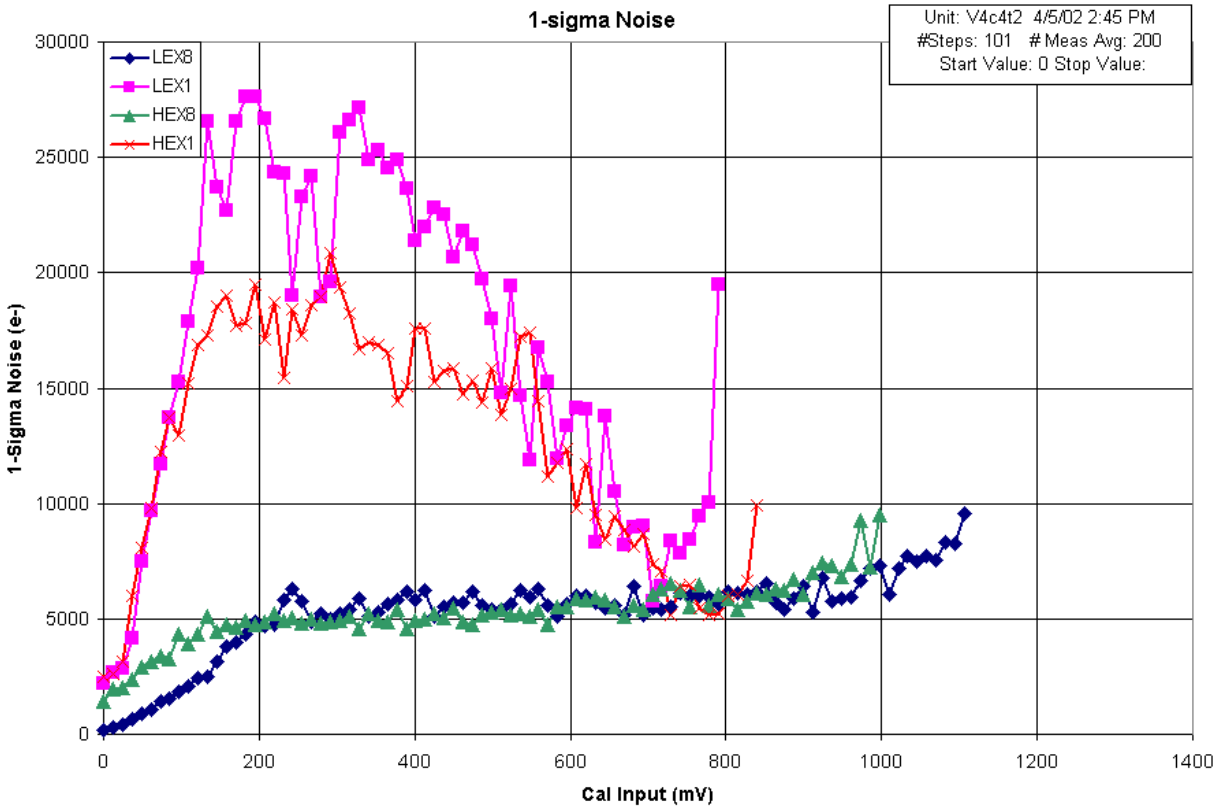


Figure 2: Version 5 SN 1 ADC Noise Meas (1-sigma)

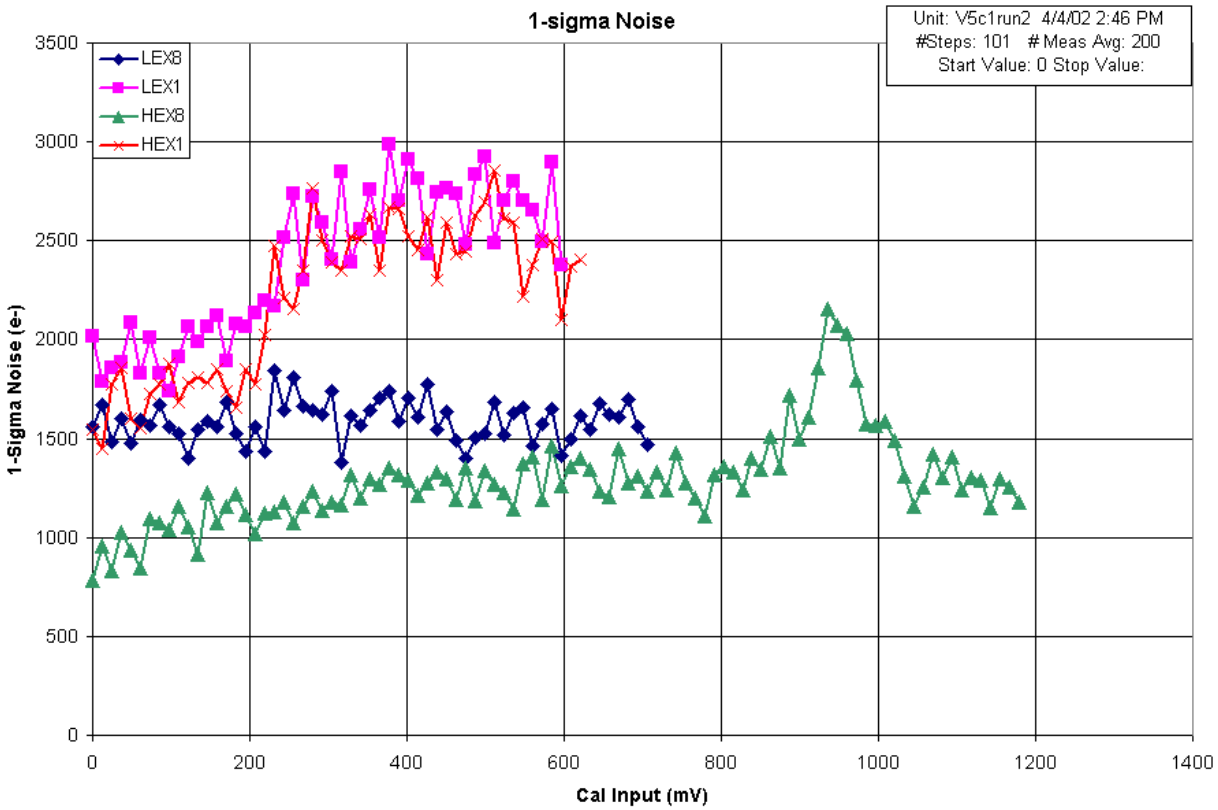
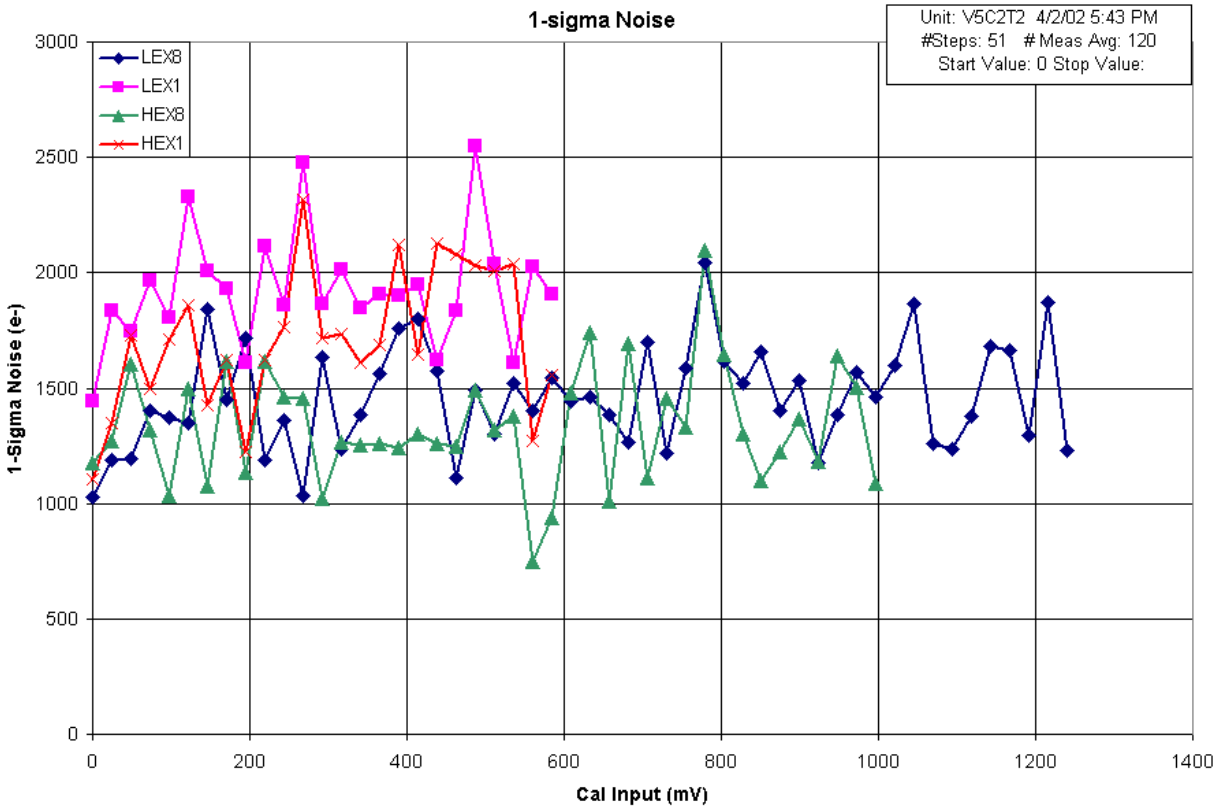


Figure 3: Version 5 SN 2 Noise Meas (1-sigma)



Additional noise measurements were also made of the slow shaper output and the Analog out signals of both the Version 4 and Version 5 ASICs. These results are shown in scope snaps below. The following 6-sigma noise measurements were observed that show a marked improvement in the noise of the X8 channels with the version 5 design.

Table 1: Slow Shaper and Analog Output Noise

	Slow Shaper Signal		Analog Out Signal	
	Version 4	Version 5	Version 4	Version 5
LEX1	12 mV	12 mV	18 mV	18 mV
LEX8	12 mV	12 mV	90 mV	28 mV

Figure 4: Scope Snap Ver 4 chip 3 LEX1 w ADC enabled

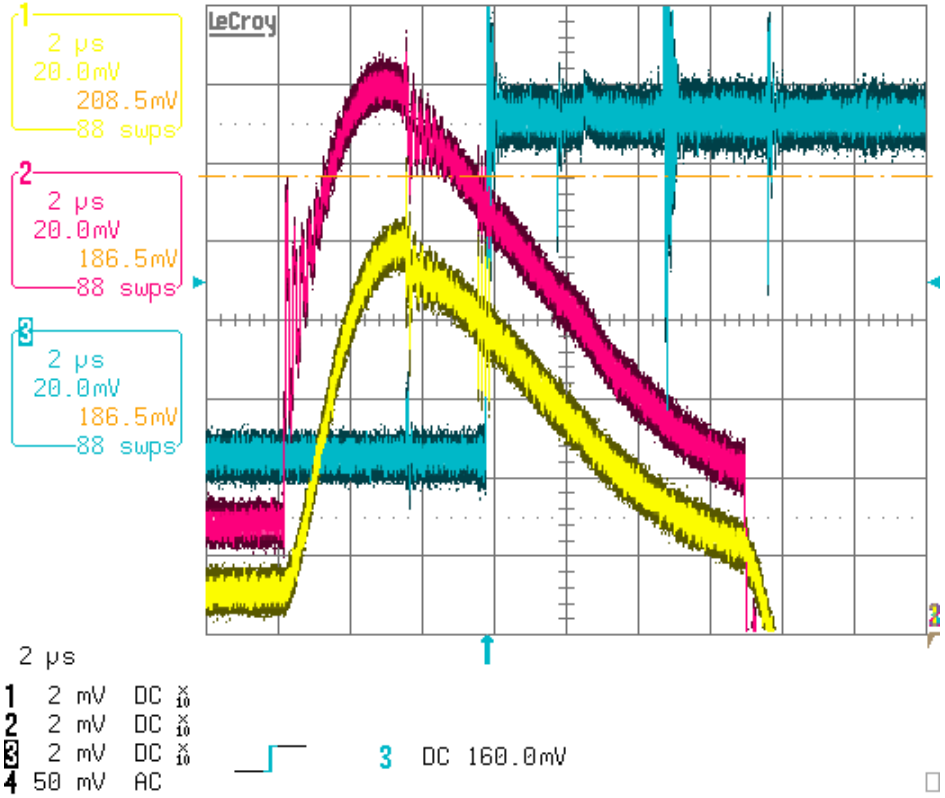


Figure 5: Scope Snap Ver 5 chip 2 LEX1 w ADC enabled

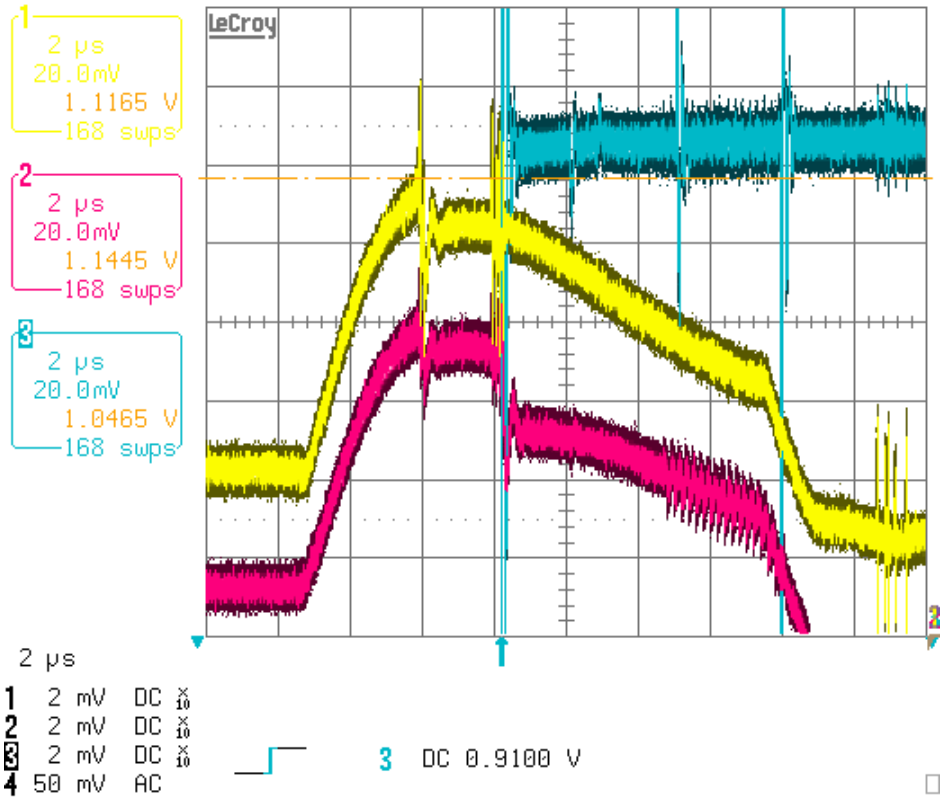


Figure 6: Scope Snap Ver 4 chip 3 LEX8 w ADC enabled

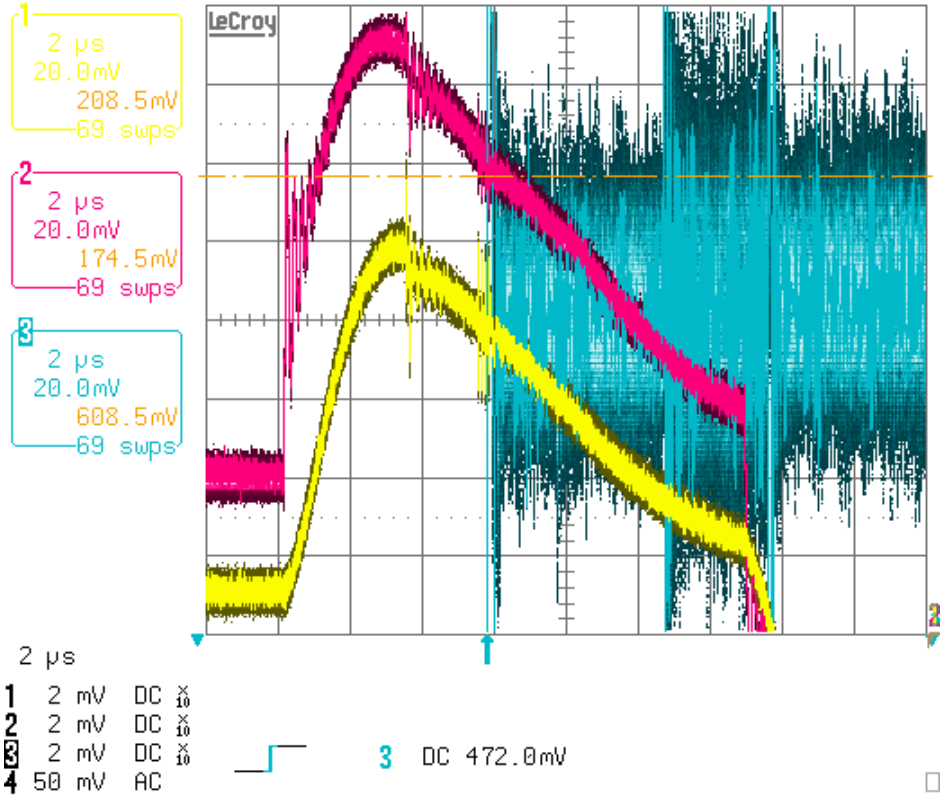


Figure 7: Scope Snap Ver 5 chip 2 LEX8 w ADC enabled

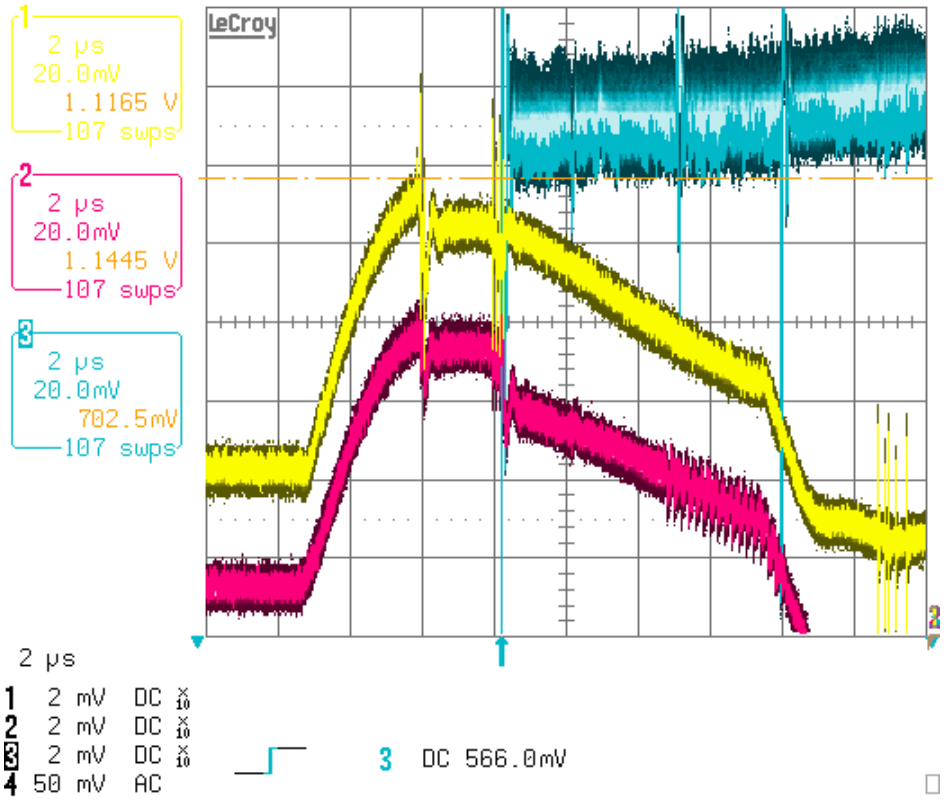


Figure 8: Scope Snap Ver 4 Chip 3 LEX8 with ADC disabled

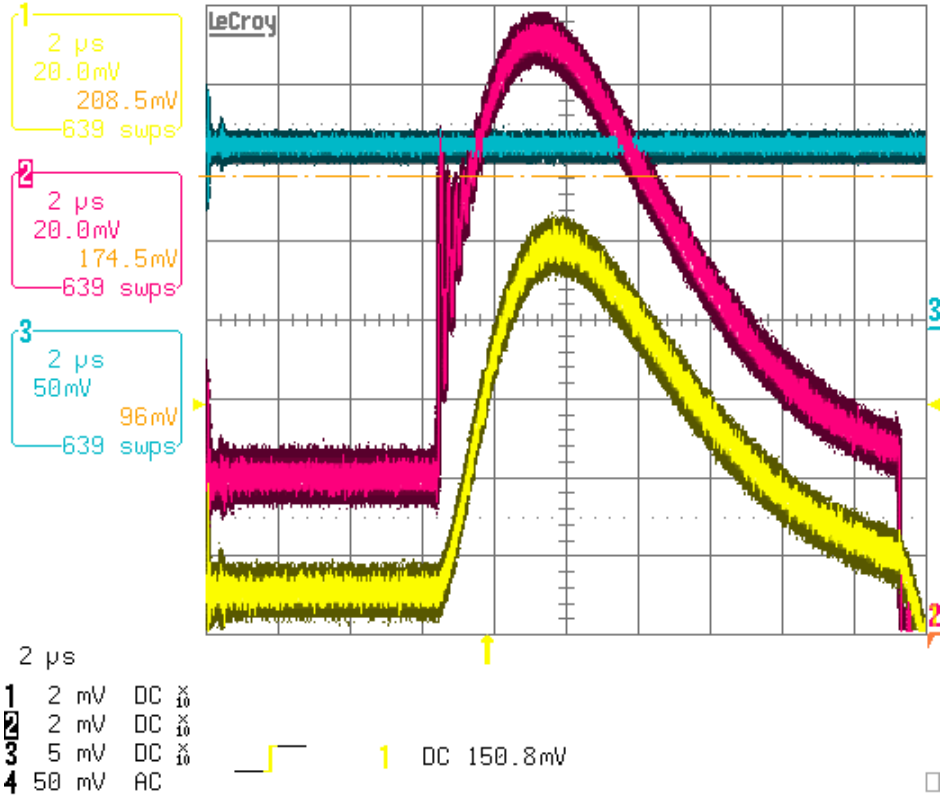
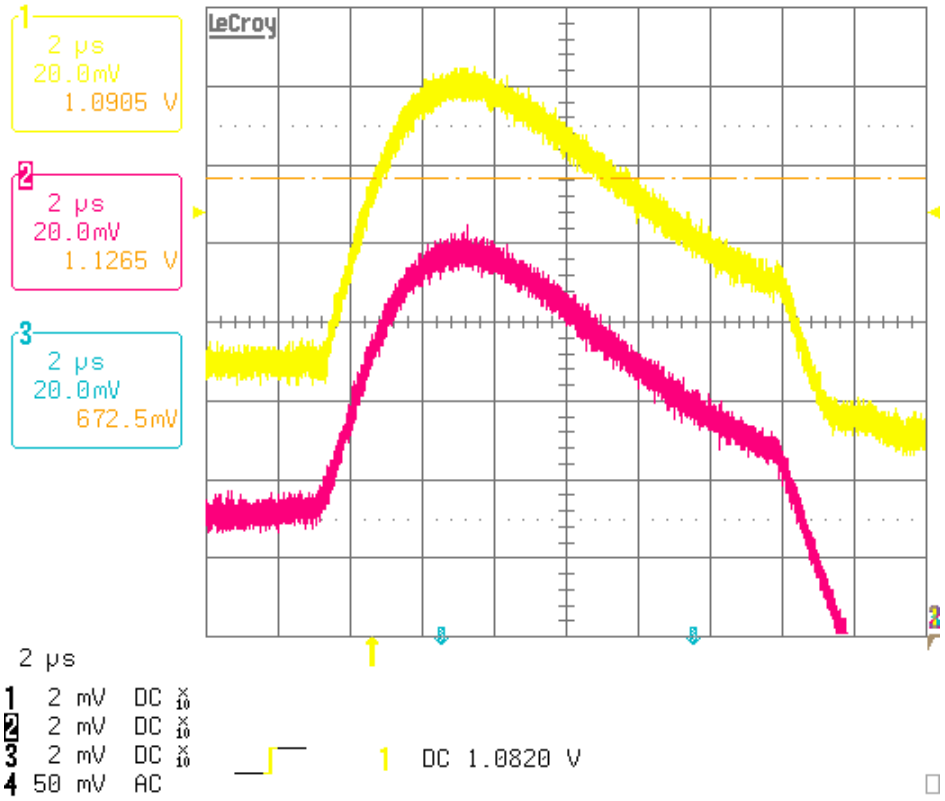


Figure 9: Scope Snap Ver 5 Chip 2 LEX8 with ADC disabled



Integral Non-Linearity Measurements:

Integral Non-linearity measurements are made by fitting a linear estimate to the ADC output signal in MeV to the Calibration Input Signal in MeV, calculating the percentage error of the measured value to the linear estimate over the measured Energy Range. The linearity is calculated over the range from 0 signal input through to just prior to saturation. This may include points under the intended threshold for that range. This can be taken into consideration when interpreting the plots of the higher-energy channels.

Figure 10: Version 4 Integral Linearity

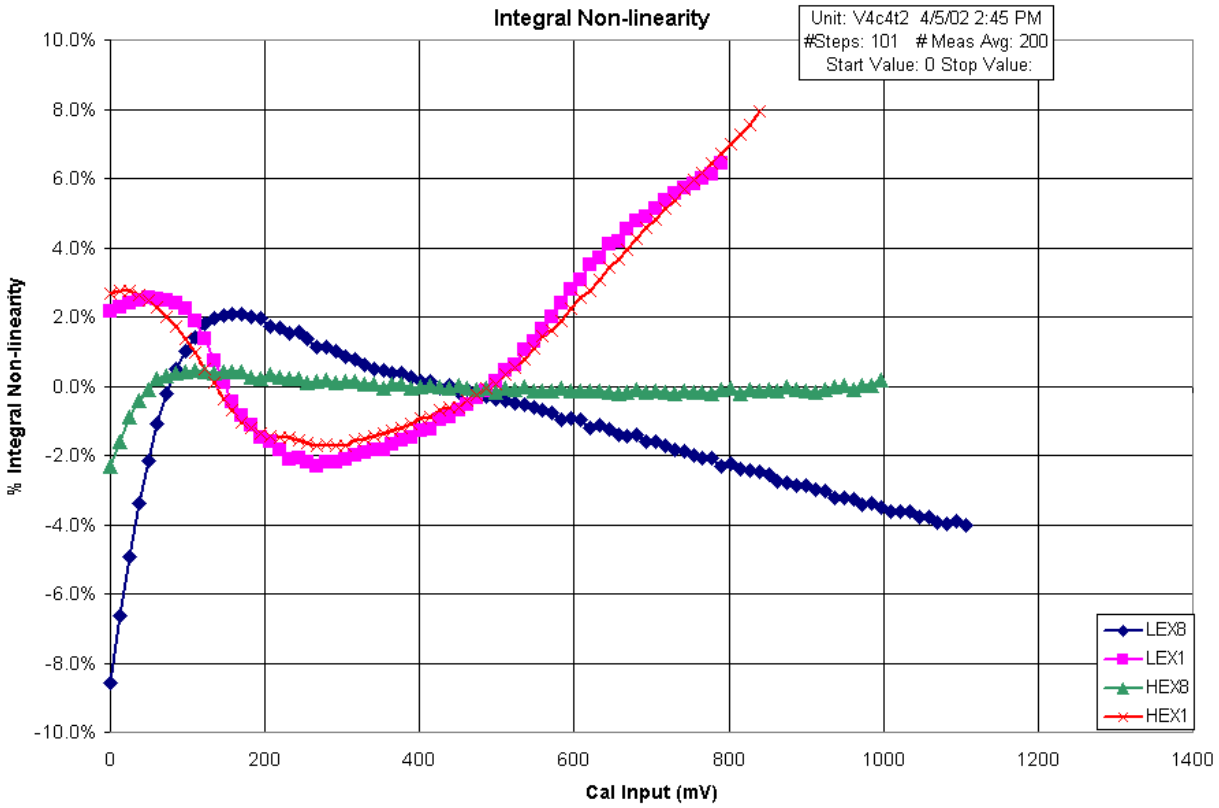


Figure 11: Version 5 SN 1 Integral Linearity

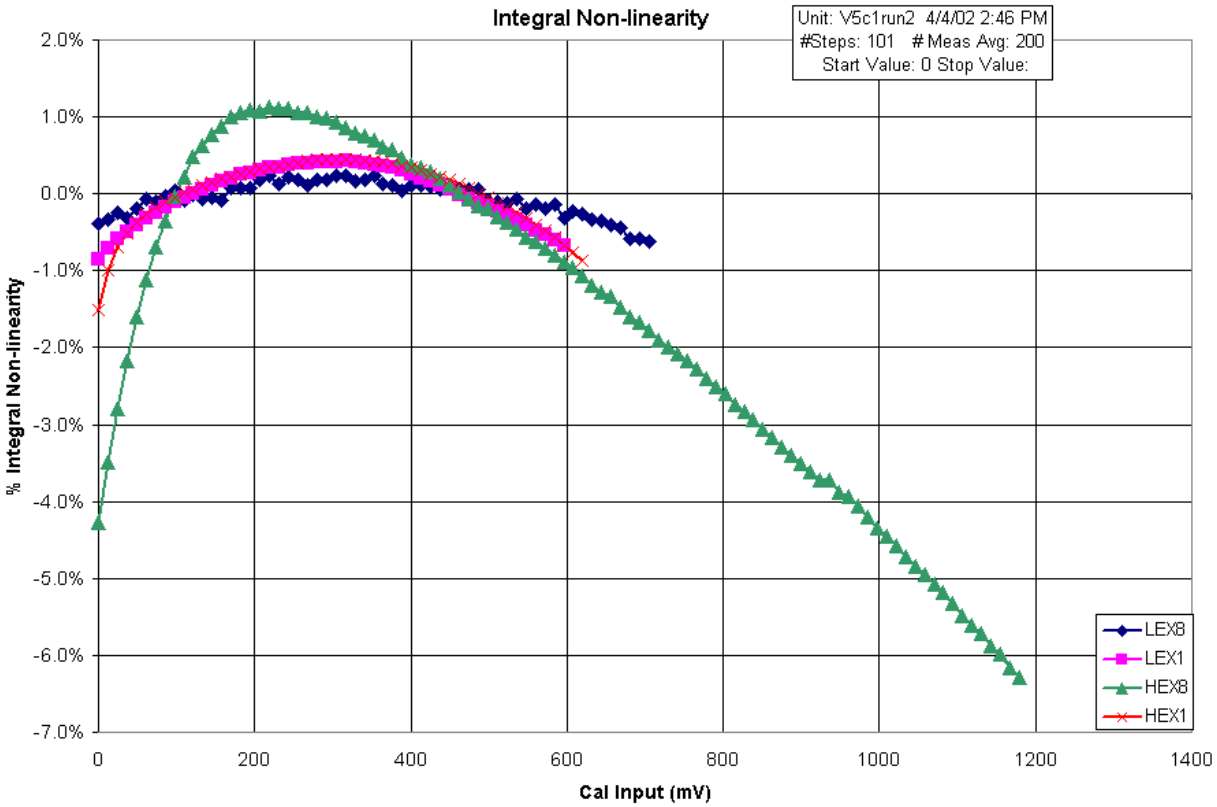
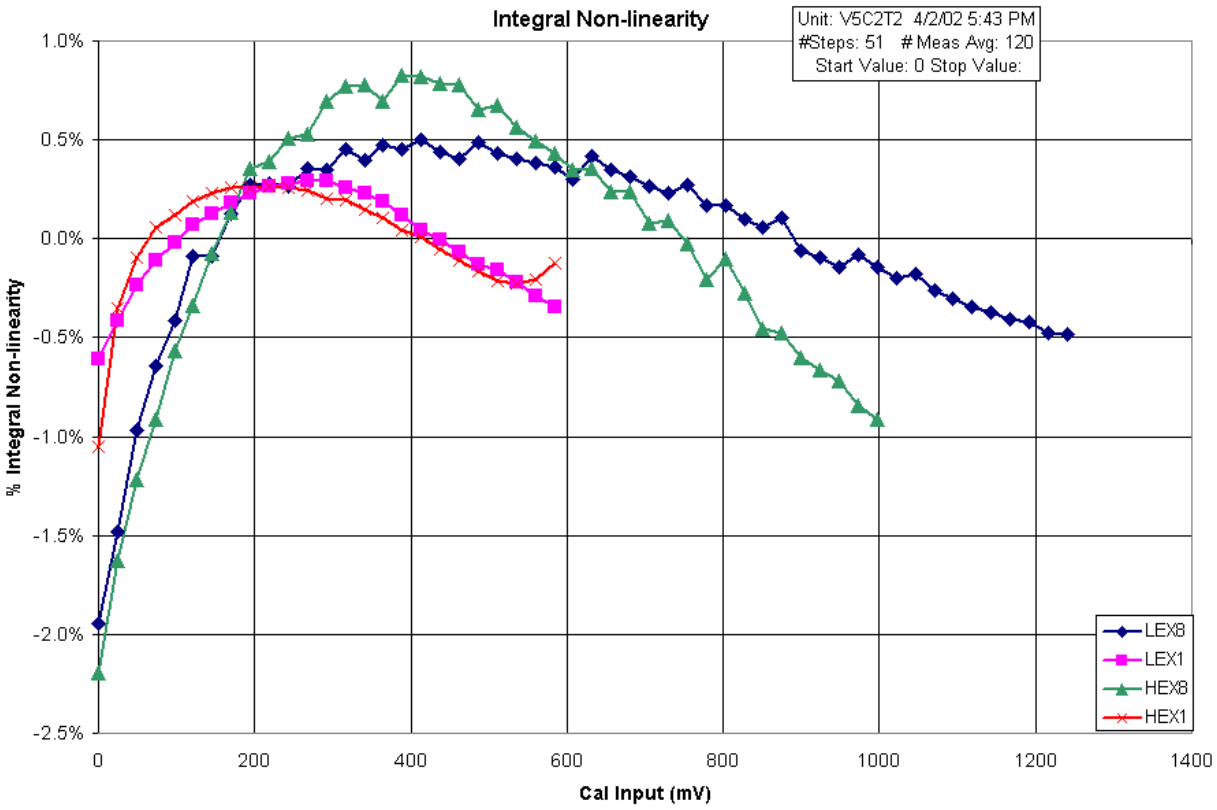


Figure 12: Version 5 SN 2 Integral Linearity



Energy Range:

The Energy Range measurements are shown below. The additional bias current required for the functionality of the Version 5 chip heavily effects these measurements. My calculations for the High Energy channels show them well below the design goal, similar to as reported in the Version 4 test report.

Figure 13: Version 4 Energy Range

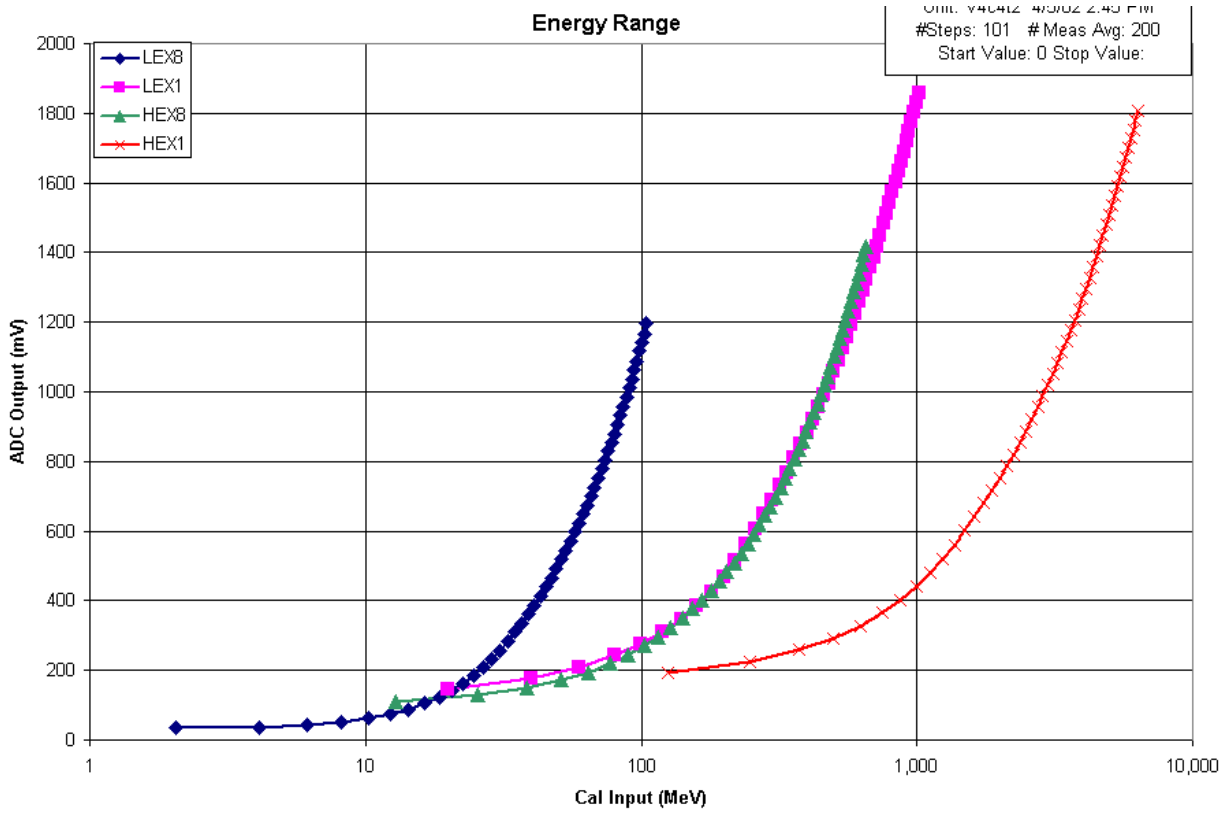


Figure 14: Version 5 SN 1 Energy Range

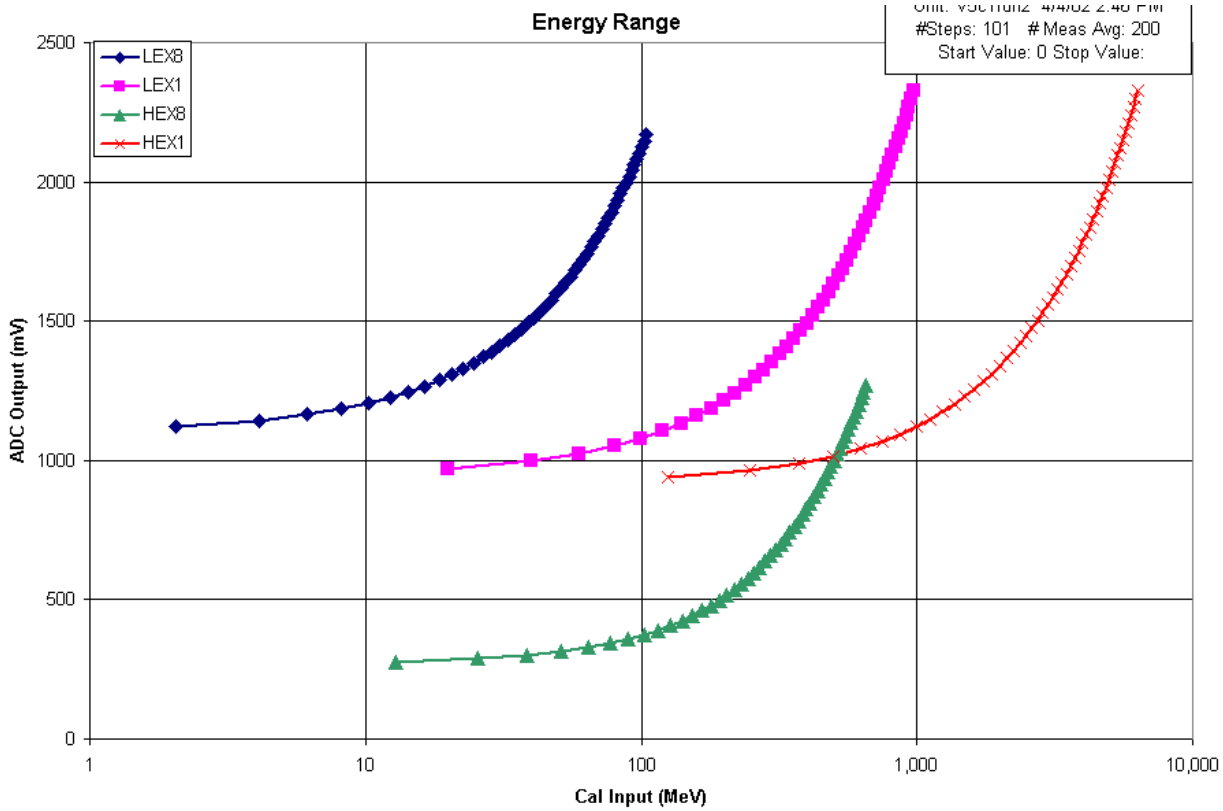
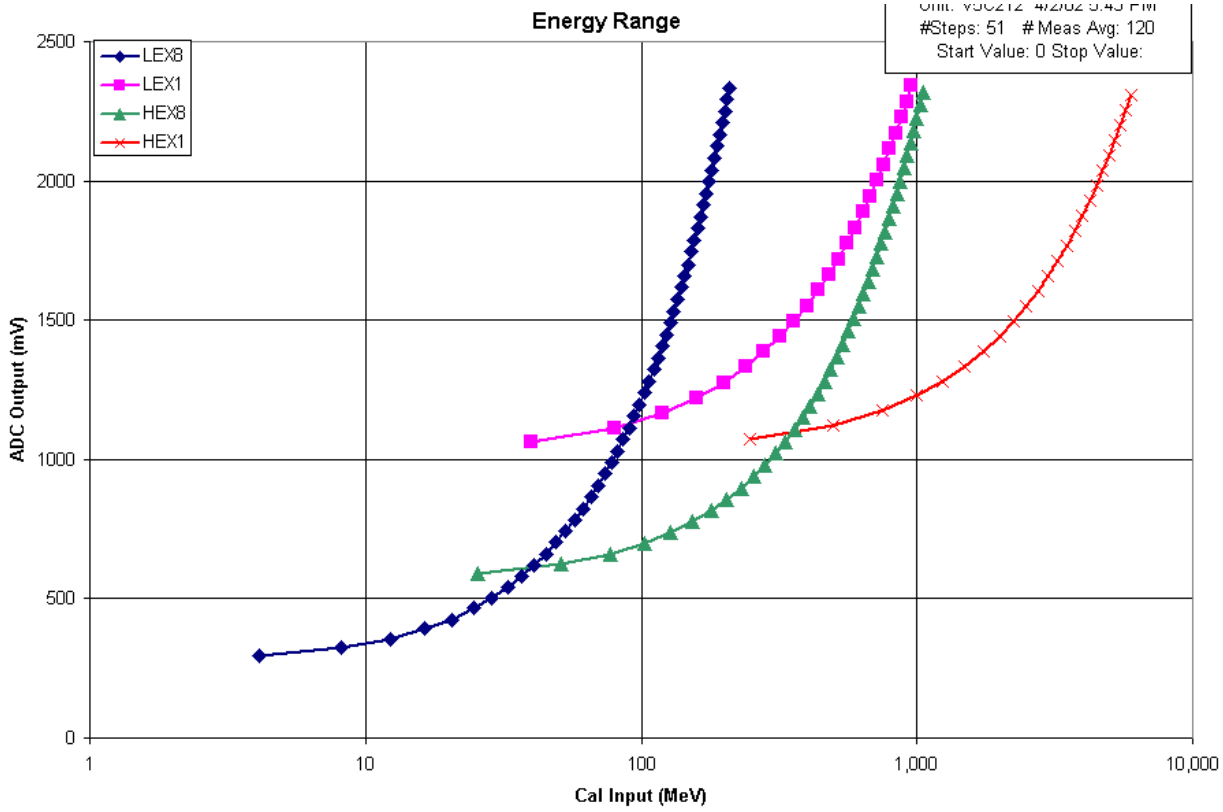


Figure 15: Version 5 SN 2 Energy Range

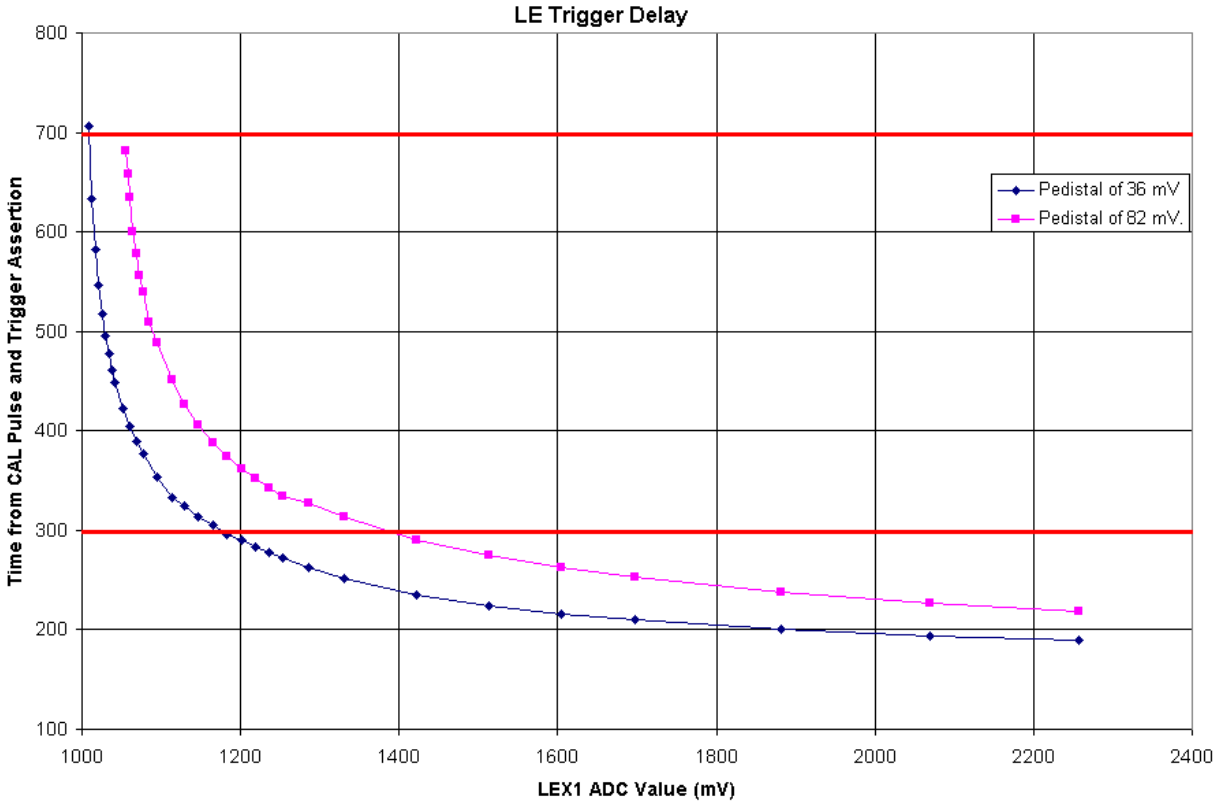


Fast Shaper Trigger Delay

The time from the calibration strobe to the fast shaper discriminator transition was measured on a scope for the full range of input signals. Two different FLE_DAC settings were measured, one with a minimum threshold voltage and a second with a higher threshold. The specification calls for this time to be 0.5 +/- 0.2 usec for all chips. The time ranged from 0.70 µsec for small pulses to as fast as 0.19 µsec for large input pulses.

The high-energy trigger timing could not be measured since, as mentioned above, the high-energy trigger was continuously triggering when enabled.

Figure 16: Low Energy Trigger Delay Measurements



Slow Shaper Peak Delay:

Slow shaper peak delay measurements have not been explicitly completed on the version 5 ASICs. The slow shaper peak does appear to have very similar timing to the version 4 chips for which it was measured to be between 3.4 and 3.75 µsec with a slightly increasing time-to-peak as the signal size increased. An efficient method to take these measurements is under development and once complete these measurements will be made over a sample of chips.

Pre-Amp Gains:

The slope of the input calibration signal magnitude to the output X1 channel ADC value was measured for each of the pre-amp gain selections. The results are shown in the table below.

The design gain values are intended for the gain from the pre-amp component alone so direct 1-1 comparison is not intended but a general agreement is observed.

Table 2: Pre-Amp Gain Measurements

	Measured slopes		Design Value (V)	
	LEX1	HEX1	LE	HE
Gain 0	5.98	20.74	4.41	15.24
Gain 1	4.57	9.43	3.12	6.27
Gain 2	3.68	6.05	2.42	3.95
Gain 3	3.09	4.46	1.97	2.88
Gain 4	2.64	3.57	1.68	2.27
Gain 5	2.32	2.96	1.45	1.87
Gain 6	2.07	2.52	1.28	1.59
Gain 7	1.86	2.19	1.14	1.39
Gain 8		6.68		4.35
Gain 9		4.79		3.09
Gain 10		3.73		2.4
Gain 11		3.06		1.96
Gain 12		2.62		1.65
Gain 13		2.27		1.43
Gain 14		2.00		1.26
Gain 15		1.79		1.13

Power Consumption:

Power consumption measurements were not complete on the Version 5 chips since the additional bias current required to operate these chips creates an obvious violation of this specification.

Conversion from mV to MeV and e-:

The following conversions are made in the spreadsheets to convert the values reported:

Conversion for Calibration Pulse:
The capacitance for the calibration pulse was not re-measured but is assumed to the same as on the Version 4 ASIC. For version 4, it was determined to be 0.135 pF with the calibration gain disabled and 1.31 pF with the calibration gain enabled.

MeV/VoIt = Capacitance / (Coulombs/Electrons * Electrons/MeV)

Where	Coulombs/Electrons		1.60 e -19
	Electrons / MeV	LE	5000
		HE	800

Resulting in the following conversion factors:

LE Cal Gain = 0	168 MeV/Volt
LE Cal Gain = 1	1637 MeV/Volt
HE Cal Gain = 0	1054 MeV/Volt
HE Cal Gain = 1	10230 MeV/Volt